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DIGITAL/ANALOG CONVERTER

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[There are no amendments to this patent.]

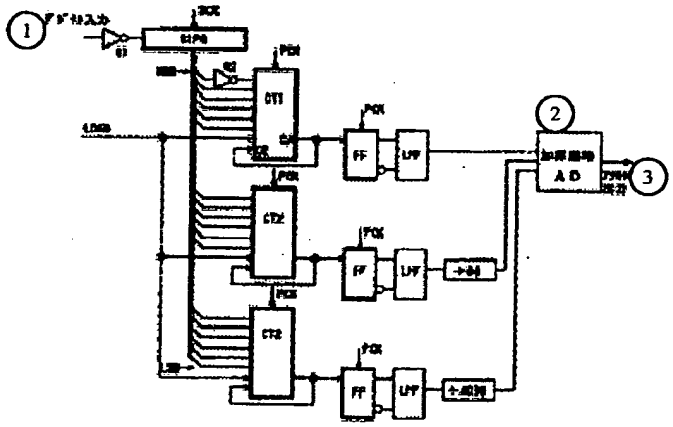
Abstract

Objective

The objective is to realize a digital/analog conversion circuit that has high performance and high stability, as well as high quality, by directly performing 1 bit digital/analog conversion of digital data without using a delta-sigma modulation method.

Constitution

N bits of digital data are divided into m groups, the width or density of pulse signals having a fixed amplitude according to a data value that can be obtained in that range is changed and modulated by means of time control. Digital/analog conversion is performed by weighting signals after modulation in divided group units and then synthesizing the output signals.



Key: 1 Digital input
2 Addition circuit
3 Analog output

Claim

A digital/analog converter characterized in that it performs digital/analog conversion by dividing N bits of digital data in m groups, changing the width or density of pulse signals having a fixed amplitude according to a data value that can be obtained in that range and modulating, weighting the signals after modulation in divided group units, and synthesizing.

Detailed explanation of the invention

[0001]

Industrial application field

The present invention relates to a digital/analog converter in various types of digital audio equipment.

[0002]

Prior art

Conventional high-precision digital/analog converters include 1 bit digital/analog converters that use a delta-sigma modulation method. They convert digital data to a fixed

amplitude pulse width or pulse density. Because the pulse width or density is generated by a digital circuit according to a high-precision timing generation circuit (clock), extremely high-precision, high-stability digital/analog conversion is realized.

[0003]

However, this does not mean that a delta-sigma converter directly converts digital data into a pulse width or density. Using the example of a CD player, for direct conversion, the number of bits quantized is 16, the sampling frequency is 44.1 kHz, and 2^{16} (= 65536) control cycles will be required in a time of 22.6757 μs (1/44.1 kHz). If pulse width conversion is considered, a timing generation circuit that will go up to

$$44.1\,\mathrm{kHz} \times 2^{16} = 2.89\,\mathrm{GHz}$$

and a logic circuit that can operate at that speed will be required, which is unrealistic.

[0004]

Basically, digital/analog converters use a very low numeric of bits (1-4 bits) and because the resolution is thereby low, the quantization noise produced is passed through a delay element and returned to the input part, so that improved resolution in the audible band is achieved by concentrating the frequency distribution of the quantization noise in the high frequency region. The operation is usually carried out at a clock speed of tens of MHz. In other words, it is a configuration that works to always correct error components produced by the low-resolution digital/analog converter. With static characteristics at fixed frequency as described above, high performance is exhibited. However, because previous error components are always returned, output containing dynamic characteristics, for example, a single digital zero, cannot be tracked immediately and is generated as noise (hunting phenomenon). In terms of sound quality, this is undesirable.

[0005]

Problems to be solved by the invention

The problem for the present invention is to realize a digital/analog converter that has high performance and high stability, as well as high quality, by directly performing 1 bit digital/analog conversion of digital data without using a delta-sigma modulation method.

[0006]

Means to solve the problems

To solve the problem described above,

[0007]

the digital/analog converter according to the present invention is characterized in that it realizes digital/analog conversion by dividing N bits of digital data into m groups, changing the width or density of pulse signals having a fixed amplitude according to a data value (2 m) that can be obtained in that range and modulating, weighting the signals after modulation in divided group units, and synthesizing.

[0008]

Function and effects of the invention

N bits of digital data from a digital signal processing circuit are divided into m groups and the number of combinations of digital data that can be obtained is reduced. Then the digital data are directly modulated to a pulse width or density with fixed amplitude in units of divided groups, the signals in each group after modulation are weighted according to the division and synthesized.

[0009]

A 1-bit digital/analog converter in which the hunting phenomenon will not occur can be thereby configured, and a digital/analog converter with high quality, as well as high precision and high stability, compared with a conventional 1-bit digital/analog converter that uses delta-sigma modulation, can be realized.

[0010]

Application example

An application example of the present invention will be explained below based on the attached figure.

[0011]

Application example (Figure 1)

This application example concerns a digital/analog converter pertaining to the present invention.

[0012]

Figure 1 is an example in which an 18-bit digital signal from a digital signal processing circuit (including a digital filter circuit) is divided into 3 groups and directly pulse-width modulated.

[0013]

The polarity serial digital data from a digital signal processing circuit (not shown) are inverted by gate (G1) and collected in a SIPO (serial-in, parallel-out) register. The shift clock BCK of the SIPO register in this case need only be several times the number of bits of the sampling frequency.

[0014]

The data placed in the SIPO register with each sampling pulse are next placed by a LOAD signal in 3 sets of 6 bit binary counter circuits (CT1)-(CT3) in parallel. Only the most significant bit MSB is polarity inverted and placed there, and a count increment operation is started by a counter clock PCK. In this case, the carry out signal CA of each counter circuit is a signal in the form of 6 bits and produces a logical "1" when all are "1," and produce the pulse-width modulation output signal. The carry out signals CA are also connected to the count enable input signal CE of the counter circuits and function as control signals to stop the count operation when the input logic of count enable input signal CE is "1."

[0015]

For example, when the original 6-bit signal for binary counter circuit (CT3) is 000011, the data collected in the SIPO register becomes 111100 because of gate (G1) and is loaded into binary counter circuit (CT3). In this case, the output for the carry out signal CA by binary counter circuit (CT3) will be "0." The count increment operation caused by counter clock PCK is enabled by the input of count enable input signal CE simultaneously being "0." [The data] change

$$111100 \rightarrow 111101 \rightarrow 111110 \rightarrow 111111$$

and simultaneously, the carry out signal CA also changes

$$0 \rightarrow 0 \rightarrow 0 \rightarrow 1.$$

The subsequent counter operation is stopped by count enable input signal CE also becoming "1" at the point when the carry out signal CA becomes "1."

[0016]

That is, carry out signal CA will always be kept at "1" until a LOAD pulse is input. With the example described above, a "0" level in the 3rd cycle by counter clock PCK is obtained by input of 000011 ("3" in decimal).

[0017]

The carry out signal CA will output a pulse with the "0" level for the 0-63rd cycles by counter clock PCK as the width corresponding to the 6-bit digital value in the manner described

above, and pulse width modulation is implemented. Thus, counter clock PCK need only be at least 64 times the sampling frequency.

[0018]

Note that the purpose of the logical inversion of the most significant bit MSB by gate (G2) is that digital audio code format is the two's complement representation. In order to avoid phase conversion, the most significant bit MSB is inverted for conversion into offset binary.

[0019]

In Figure 1, (CT1)-(CT3) use increment counters, but it goes without saying that they can be changed to decrement counters, and the function described above can be realized with a similar circuit configuration by leaving out gate (G1). Also, with Figure 1, the case of division into 6 bits was illustrated, but, needless to say, the number of bits in the division is determined according to the speed at which the clock can operate on the basis of the circuit configuration.

[0020]

The 3 sets of pulse-width modulated output obtained as described above undergo waveform-shaping by flip-flop FF, are then passed through low-pass filter LPF for weighting corresponding to the individual group, and are then synthesized by addition circuit AD. With the example in Figure 1, because the data are divided into 3 groups of 6 bits, when weighting of the most significant group is x1, the weighting of the middle group will be x (1/64) and the weighting of the least significant group will be x (1/04096).

[0021]

The output can also be easily produced according to the logical value of carry out signal CA and counter clock PCK even when modulating with pulse density rather than with pulse-width modulation.

[0022]

In the present invention as described above, it is possible to configure a 1-bit digital/analog converter in which the hunting phenomenon will not occur, and it is possible to realize digital/analog conversion with high quality, as well as high precision and stability, compared with a conventional 1-bit digital/analog converter that uses delta-sigma modulation.

Brief description of the figure

Figure 1 is a block diagram of a digital/analog converter pertaining to the present invention in an application example.

Explanation of the symbols

SIPO	SIPO (serial-in, parallel-out) register
G1, G2	Gates
CT1, CT2, CT3	Binary counter circuits
BCK	Shift clock
PCK	Counter clock
CA	Carry out signal
CE	Counter enable signal
FF	Flip-flop
LPF	Low-pass filter
AD	Addition circuit
MSB	Most significant bit
LSB	Least significant bit

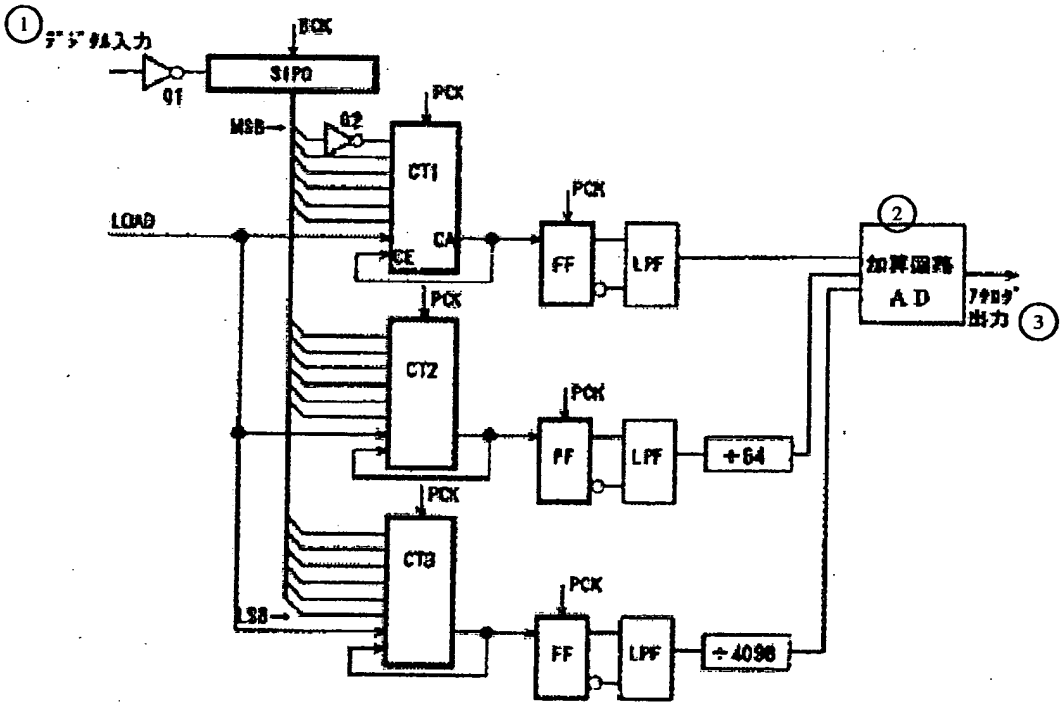


Figure 1

Key: 1 Digital input

2 Addition circuit
3 Analog output

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To Whom It May Concern:

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We certify that the attached English translation conforms essentially to the original Japanese language.

Kim Vitray
Operations Manager

Subscribed and sworn to before me this 20th day of April, 2005.

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